In the Claims:

The pending claims are presented below.

1. (Original) A parallel data communication arrangement susceptible to skewing data, comprising:

a parallel bus having parallel bus lines adapted to transfer digital data, the parallel bus lines being arranged in a plurality of groups wherein each group includes a plurality of data-carrying lines and a clock path adapted to carry a clock signal for synchronizing digital data carried over the plurality of data-carrying lines of the group;

a first module adapted to transfer sets of data concurrently on the plurality of groups of lines of the parallel bus; and

a second module adapted to collect, for each group, the digital data carried from the first module over the plurality of data-carrying lines as synchronized by the clock signal for the group and adapted to align the data collected for each group and overcome any skew-caused misalignments between data concurrently transferred in different groups.

2. (Original) The parallel data communication arrangement of claim 1, wherein for each group the clock path is implemented using a pair of the parallel bus lines, the pair of the parallel bus lines adapted to carry the clock signal as a differential signal.

3. (Original) The parallel data communication arrangement of claim 2, wherein for each group, data carried by the plurality of data-carrying lines are synchronized by the differential clock signal to tolerate any skew-caused misalignments between data concurrently transferred in the group, the skew-caused misalignments not exceeding one half clock period.

4. (Original) The parallel data communication arrangement of claim 1, wherein for each group, data carried by the plurality of data-carrying lines are synchronized by the clock signal to tolerate any skew-caused misalignments between data concurrently transferred in the group, the skew-caused misalignments not exceeding one half clock period.

5. (Original) The parallel data communication arrangement of claim 1, wherein the clock signal is a differential clock signal, and the first and second modules are further adapted to

process concurrent data to permit the second module to resolve for each group, data carried by the plurality of data-carrying lines and the differential clock signal within a single clock period of the clock signal, thereby tolerating a certain degree of skew-caused misalignments.

6. (Original) The parallel data communication arrangement of claim 1, wherein the first and second modules are further adapted to process concurrent data to permit for the second module to resolve for each group, data carried by the plurality of data-carrying lines and the differential clock signal within a single clock period of the clock signal, and, between data concurrently transferred in different groups, to permit skew-caused misalignments that exceed one-half clock period.

7. (Original) The parallel data communication arrangement of claim 1, wherein the data carried over the plurality of data-carrying lines is encoded, and wherein the second module includes for each group: a receiver circuit responsive to the clock signal and adapted to receive the digital data carried from the first module over the plurality of data-carrying lines, a data decoder adapted to decode the received digital data; and a FIFO buffer adapted for storing the decoded data.

8. (Original) The parallel data communication arrangement of claim 1, wherein for each group, the data decoder converts an X-bit value to a Y-bit value, where X and Y are positive integers and X is greater than Y, and wherein the Y-bit value is stored in the FIFO buffer.

9. (Original) The parallel data communication arrangement of claim 1, wherein for each group, the clock signal is used to synchronize the reception of two sets of multiple-bit data values at the receiver circuit.

10. (Original) The parallel data communication arrangement of claim 1, wherein for each group, the clock signal is used to synchronize the reception of two sets of encoded multiple-bit data values at the receiver circuit, and wherein the second module includes for each group: a data decoder adapted to decode the multiple-bit data values, and a FIFO buffer adapted to store the decoded data.

11. (Original) The parallel data communication arrangement of claim 10, wherein for each group, the data decoder converts an 8-bit value to a 6-bit value, and wherein the 6-bit value is stored in the FIFO buffer.

12. (Original) The parallel data communication arrangement of claim 10, wherein the second module further includes data processing circuitry and another FIFO buffer, the data processing circuitry and the other FIFO buffer adapted to collect the decoded data from the FIFO buffers of the respective groups, and wherein the data collected for each group is aligned after being stored in the other FIFO buffer.

13. (Original) The parallel data communication arrangement of claim 12, wherein the second module is further adapted to align the data by processing the stored multiple-bit data values, said processing including distinguishing valid multiple-bit data values from invalid multiple-bit data values.

14. (Original) The parallel data communication arrangement of claim 10, further including a feedback communication path adapted to feed information from the second module to the first module, the information indicating at least one of: an error signal indicating that too much data has been sent; and a warning signal indicating that ongoing communication is approaching a near-full condition.

15. (Original) The parallel data communication arrangement of claim 1, wherein the first module and the second module include respective circuitries for processing data over another parallel data bus for data transferred from the second module to the first module, the respective circuitries including operations that are reciprocal relative to data transferred from the first module to the second module.

16. (Original) A parallel data communication arrangement susceptible to skewing data, comprising:

a parallel bus having parallel bus lines adapted to transfer digital data, the parallel bus lines being arranged in a plurality of groups wherein each group includes a plurality of data-carrying lines and a clock path adapted to carry a clock signal for synchronizing digital data carried over the plurality of data-carrying lines of the group;

a first module including data processing circuitry adapted to arrange and encode data values to be transferred over the parallel bus and including driver circuits adapted to transfer sets of data concurrently on the plurality of groups of lines of the parallel bus; and

a second module including data processing circuitry adapted to receive and decode data values transferred from the first module over the parallel bus, the processing circuitry including a plurality of FIFO buffers each respectively assigned to one of the plurality of groups, and each FIFO buffer being adapted to collect for each group the digital data carried over the plurality of data-carrying lines as synchronized by the group clock signal, and the processing circuitry being adapted to align the data collected for each group and overcome any skew-caused misalignments between data concurrently transferred in different groups.

17. (Original) The parallel data communication arrangement of claim 16, wherein the first module and the second module include respective circuitries for processing data over another parallel data bus for data transferred from the second module to the first module, the respective circuitries including operations that are reciprocal relative to data transferred from the first module to the second module.

18. (Original) The parallel data communication arrangement of claim 16, wherein for each group, the clock signal is differential and is used to synchronize the reception of two sets of encoded multiple-bit data values at the receiver circuit, and wherein the second module includes for each group: a data decoder adapted to decode the multiple-bit data values, and a FIFO buffer adapted to store the decoded data, and wherein the second module further includes data processing circuitry and another FIFO buffer, the data processing circuitry and the other FIFO buffer adapted to collect the decoded data from the FIFO buffers of the respective groups, and wherein the data collected for each group is aligned after being stored in the other FIFO buffer.

19. (Original) The parallel data communication arrangement of claim 18, wherein the second module is further adapted to align the data by processing the stored multiple-bit data values, said processing including distinguishing valid multiple-bit data values from invalid multiple-bit data values.

20. (Original) A parallel data communication arrangement susceptible to skewing data, comprising:

a parallel bus having parallel bus lines adapted to transfer digital data, the parallel bus lines being arranged in a plurality of groups wherein each group includes a plurality of data-carrying lines and a clock path adapted to carry a clock signal for synchronizing digital data carried over the plurality of data-carrying lines of the group;

first means for transferring sets of data concurrently on the plurality of groups of lines of the parallel bus; and

second means for collecting, for each group, the digital data carried from the first means over the plurality of data-carrying lines as synchronized by the clock signal for the group and for aligning the data collected for each group and overcoming any skew-caused misalignments between data concurrently transferred in different groups.

21. (Original) A method of transferring digital data from a first module to a second module over a parallel bus having parallel bus lines susceptible to skewing data carried by the bus, the method comprising:

arranging the parallel bus lines in a plurality of groups, each of the groups including a plurality of data-carrying lines and a clock path adapted to carry a clock signal for synchronizing digital data carried from the first module to the second module over the plurality of data-carrying lines of the group;

transferring sets of data concurrently using the groups of lines of the parallel bus;

at the second module and for each group, collecting the digital data carried from the first module over the plurality of data-carrying lines as synchronized by the clock signal for the group; and

at the second module, aligning the data collected for each group and overcoming any skew-caused misalignments between data concurrently transferred in different groups.